



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,014	04/12/2001	Scott L. Jacobs	0262-005	5260

7590

10/04/2002

VIRTUAL INTEGRATION, INC
NIXON AND VANDERHYE, P.C.
1100 NORTH GLEBE RD.
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER

ANDUJAR, LEONARDO

ART UNIT PAPER NUMBER

2826

DATE MAILED: 10/04/2002

9


Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

09/834,014

Applicant(s)

JACOBS, SCOTT L. 

Examiner

Leonardo Andújar

Art Unit

2826

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) g.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 3, 5, 7-9, 11, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Tokuda et al. (US 5,870,289).

4. Regarding claim 1, Tokuda (e.g. fig. 6) shows a microelectronic package comprising:

- A first level substrate including a plurality of microelectronic devices 411 and a plurality of first level substrate input/output pads in a face thereof;
- A thin film decal 451 on the face of the first level substrate and having a first and second opposing faces;
- A second level substrate 480 including a plurality of second level substrate input/output pads on a face thereof;

- And a dielectric adhesive layer 462 adhesively bonded to the thin film decal and to the second substrate.

5. Tokuda shows that the thin film decal includes a plurality of first decal input/output pads on the first face electrically connected to first level substrate input/output pads located in the first level substrate. Also, the decal includes a plurality of second decal input/output on the second face, which are electrically connected to the first decal input/output pads by internal wiring layers 440. The adhesive layer includes a plurality of conductive vias 470 to electrically connect the second substrate input/output pads to the second decal input/output pads.

6. Regarding claim 3, Tokuda shows the first level substrate is an integrated circuit and the second level is a printed circuit board.

7. Regarding claim 5, Tokuda shows a buffer layer 463 in the dielectric adhesive layer.

8. Regarding claim 7, Tokuda shows that the first face is substantially planar and topography free.

9. Regarding claim 8, Tokuda shows that the thin film decal and the dielectric adhesive layer collectively comprises a Planar Graft Patch that is grafted onto the second level substrate form a process substrate.

10. Regarding claim 9, Tokuda (e.g. fig. 6) shows a microelectronic package comprising:

- A substrate 451-1n;
- A release layer on the substrate 461-n;

- A thin film decal 451-n on the release layer, opposite the substrate, and having a first and second opposing faces;
- And a dielectric adhesive layer 462 adhesively bonded to the thin film decal.

11. Tokuda shows that the thin film decal includes a plurality of first decal input/output pads on the first face. Also, the decal includes a plurality of second decal input/output on the second face, which are electrically connected to the first decal input/output pads by internal wiring layer 440. The adhesive layer includes a plurality of conductive vias 470 to electrically connect the second substrate input/output pads to the second decal input/output pads.

12. Regarding claim 11, Tokuda discloses that the substrate is made of glass (col. 13/lls. 44-48).

13. Regarding claim 13, Tokuda shows a buffer layer 463 in the dielectric adhesive layer.

14. Regarding claim 15, Tokuda shows that the first face is substantially planar and topography free.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2826

16. Claims 2, 4 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokuda et al. (US 5,870,289) in view of Tomura et al. (US 5,640,051).

17. Regarding claims 2 and 10, Tokuda shows most aspects of the instant invention including conductive vias 470. Tokuda does not disclose that the conductive vias comprises a conductive adhesive vias. Nonetheless, it is conventional in the art to fill the vias with conductive adhesive. Tomura (e.g. figs. 5A –5E) shows a substrate having vias 2b filled with a conductive adhesive. Moreover, the conductive adhesive serves to, as well as mechanically adhering the carrier body to the circuit substrate, electrically connect the internal conductor of the carrier body to the terminal electrodes of the circuit substrate (col.5 /lts. 43-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to fill the conductive vias disclosed by Tokuda with conductive adhesive to mechanically adhere the substrates as well as to electrically connected the internal conductors as taught by Tomura.

18. Regarding claims 4 and 12, Tokuda in view of Tomura shows that the vias are screened conductive adhesive vias.

19. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokuda et al. (US 5,870,289) in view of Frankeny et al. (US 5,121,229).

20. Regarding claims 6 and 14, Tokuda shows most aspects of the instant invention including a thin film decal substrate having a first surface. However, Tokuda does not show that the first face includes a rippled surface. Frankeny (e.g. fig. 12) shows a microelectronic substrate having a first face with a rippled surface. Also, Frankeny

discloses that this type of embodiment permits an accurate registration between the cores during its construction process. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first face of the film decal substrate disclosed by Tokuda having a rippled surface in order to provide an accurate registration between the cores as taught by Frankeny.

Conclusion

21. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **-7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

23. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900**.

24. The following list is the Examiner's field of search for the present Office Action:



Art Unit: 2826

Field of Search	Date
U.S. Class / Subclass (es): 257/782, 783 and 778	09/02
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	09/02

Leonardo Andújar

Patent Examiner Art Unit 2826

LA
9/26/02

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800_R